UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,061	11/13/2003	Kangguo Cheng	FIS9-2003-0240	6356

7590 12/14/2004

McGuireWoods LLP
Suite 1800
1750 Tysons Boulevard
McLean, VA 22102

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,061	CHENG ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

STACY A. WHITMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 9/29/04. Currently, claims 1-24 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 11/13/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugii et al., US Patent 6,723,541 in view of Forbes Patent Application Publication US 2004/0235264.

Sugii discloses the semiconductor method substantially as claimed. See figures 1-17, and corresponding text, where Sugii shows pertaining to claim 1, a method of fabricating a semiconductor structure, comprising the steps of: forming a $Si_{1-x}Ge_x$ layer **4** on a substrate **0** (figure 8; col. 12, lines 36-60); forming a plurality of channels **14** in the $Si_{1-x}Ge_x$ layer and the substrate (figure 10; col. 12, lines 61-67); filling the channels with a dielectric material (figure 11; col. 13, lines 1-2). In addition, Sugii shows, pertaining to claim 2, a method wherein: the substrate includes a first silicon layer **3**, a second insulator layer **2** and a third substrate layer **3**; the plurality of channels include at least a first channel and a second channel extending through the $Si_{1-x}Ge_x$ layer to the bottom of the first silicon layer of the substrate (figure 10; col. 12, lines 61-67). Also, Sugii shows, pertaining to claim 7, further comprising a step of annealing the $Si_{1-x}Ge_x$ layer (col. 4, lines 19-25). Sugii shows, pertaining to claim 8, wherein the step of forming the $Si_{1-x}Ge_x$ layer includes a step from the group consisting of: ultrahigh vacuum chemical vapor deposition (UHVCVD) (col. 10, lines 5-8); rapid thermal chemical vapor deposition (RTCVD); low-pressure chemical vapor deposition (LPCVD) (col. 12, lines 45-51); limited reaction processing CVD (LRCVD); and molecular beam (MBE). Sugii shows, pertaining to claim 9, Sugii shows, further comprising a step of forming a cap layer **6/12/13** a top the $Si_{1-x}Ge_x$ layer (figure 9; col. 12, lines 57-60). Sugii shows, pertaining to claim 10, further comprising the steps of: removing the cap layer (figure 14; col. 13, lines 7-10); and forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer (figure 16; col. 13, lines 14-17). In addition, Sugii shows, pertaining to claim 11, further comprising a step of thickening the $Si_{1-x}Ge_x$ layer by forming a second $Si_{1-x}Ge_x$ layer of the first $Si_{1-x}Ge_x$ layer (col. 12, lines 51-55). Also, Sugii shows, pertaining 12, further comprising a step of forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer (figure

16, col. 13, lines 14-17). Sugii shows, pertaining 13, wherein the step of forming the strained semiconductor layer is a step from the group consisting of: ultrahigh vacuum chemical vapor deposition (UHVCVD); rapid thermal chemical vapor deposition (RTCVD); low-pressure chemical vapor deposition (LPCVD) (col. 13, lines 14-17); limited reaction processing CVD (LRPCVD); and molecular beam epitaxy (MBE). In addition, Sugii shows, pertaining to claim 14, wherein the strained semiconductor layer is comprised of a semiconductor from a group consisting of Si and $Si_{1-y}C_y$ (col. 13, lines 14-17 strained Si). Finally, Sugii shows, pertaining to claim 15, further comprising a step of forming a device on the semiconductor structure between the first and second channels as filled with dielectric material (figure 11; col. 13, lines 1-2).

Sugii shows pertaining to claim 16, a method of fabricating a semiconductor structure, comprising the steps of: forming a $Si_{1-x}Ge_x$ layer on a silicon-on-insulator substrate having a first silicon layer, a second SiO_2 layer and a third substrate layer (figure 8; col. 12, lines 36-60); forming a first channel and a second channel, each channel extending through the $Si_{1-x}Ge_x$ layer to the bottom of the first silicon layer of the substrate, the first channel and second channel being substantially parallel (figure 10; col. 12, lines 61-67); filling the first and second channels with a dielectric material (figure 11; col. 13, lines 1-2); forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer (col. 13, lines 14-17 strained Si). In addition, Sugi shows, pertaining to claim 17, a method further comprising a step of thermal annealing the $Si_{1-x}Ge_x$ layer (col. 4, lines 19-25). Also, Sugi shows, pertaining to claim 18, a method further comprising a step of planarization after filling the first and second channels with dielectric material (col. 13, lines 7-8). Sugii shows, pertaining to claim 19, a method wherein the step of forming the $Si_{1-x}Ge_x$ layer is a step from the group consisting of: ultrahigh vacuum chemical vapor deposition (UHVCVD) (col. 10,

lines 5-8); rapid thermal chemical vapor deposition (RTCVD); low-pressure chemical vapor deposition (LPCVD); limited reaction processing CVD (LRCVD); and molecular beam (MBE). In addition, Sugii shows, pertaining to claim 20, a method wherein the step of forming the strained semiconductor layer is a step from the group consisting of: ultrahigh vacuum chemical vapor deposition (UHVCVD); rapid thermal chemical vapor deposition (LPCVD); low-pressure chemical vapor deposition (LPCVD) (col. 12, lines 45-51); limited reaction processing CVD (LRPCVD); and molecular beam epitaxy (MBE). Also, Sugii shows, pertaining to claim 21, a method further comprising a step of forming a cap layer a top the $Si_{1-x}Ge_x$ layer (figure 9; col. 12, lines 57-60). Sugii shows, pertaining to claim 22, a method further comprising the steps of: removing the cap layer (figure 14; col. 13, lines 7-10); and forming a strained semiconductor layer on the $Si_{1-x}Ge_x$ layer (figure 16; col. 13, lines 14-17). In addition, Sugi shows, pertaining to claim 23, a method wherein the step of forming a strained semiconductor layer includes a step from the group consisting of: epitaxially growing a strained Si layer (figure 16; col. 13, lines 14-17); and epitaxially growing a strained $Si_{1-y}C_y$ layer. Finally, Sugii shows, pertaining to claim 24, a method further comprising a step of forming a device on the semiconductor structure between the first and second channels as filled with dielectric material (figure 11; col. 13, lines 1-2).

However, Sugii fails to show, pertaining to claims 1 and 16, removing a portion of the substrate (silicon layer) underneath the $Si_{1-x}Ge_x$ layer to form a void in the substrate (first silicon layer of the substrate from the first channel to the second channel); and filling the channels (first and second channels) and the void with a dielectric material. In addition, Sugii fails to show, pertaining to claim 2, wherein, the void is formed in the first silicon layer of the substrate

underneath the $Si_{1-x}Ge_x$ layer extending from at least the first to the second channel. Also, pertaining to claim 3, Sugii fails to show, a method wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer includes a step from the group consisting of: etching the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the substrate than for $Si_{1-x}Ge_x$; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant from the group consisting of ammonia, tertramethyl ammonium hydroxide, nitric acid and hydrofluoric acid. Sugii fails to show, pertaining to claim 4, a method wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface. In addition, Sugii fails to show, pertaining to claim 5, a method wherein the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface. Also, Sugii fails to show, pertaining to claim 6, a method wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer to form a void in the first silicon layer of the substrate from the first channel to the second channel produces a relaxed portion of the $Si_{1-x}Ge_x$ layer above the void. Sugii fails to show, pertaining to claims 7 and 17, a method further comprising a step of (thermal) annealing the $Si_{1-x}Ge_x$ layer after the void is formed in the first silicon layer (and before the first and second channels and the void are filled with dielectric material). Finally, Sugi fails to show, pertaining to claim 18, a method further comprising a step of planarization after filling the first and second channels and the void with a dielectric material.

Forbes teaches, in figures 1-16, and corresponding text, a similar method of fabricating of a semiconductor structure, pertaining to claims 1 and 16, removing a portion of the substrate (silicon layer) underneath the $Si_{1-x}Ge_x$ layer to form a void in the substrate (first silicon layer of the substrate from the first channel to the second channel) (figures 8A-8E; paragraphs [0045-0049]); and filling the channels (first and second channels) and the void with a dielectric material (figure 8E; paragraphs [0048-0049]). In addition, Forbes teaches, pertaining to claim 2, wherein, the void is formed in the first silicon layer of the substrate underneath the $Si_{1-x}Ge_x$ layer extending from at least the first to the second channel (figure 8E; paragraphs [0048-0049]). Also, pertaining to claim 3, Forbes teaches, a method wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer includes a step from the group consisting of: etching the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer (figure 8D; paragraph [0048]); performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the substrate than for $Si_{1-x}Ge_x$; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant from the group consisting of ammonia, tertramethyl ammonium hydroxide, nitric acid and hydrofluoric acid. Forbes teaches, pertaining to claim 4, a method wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface (paragraph [0034] and [0049]). In addition, Forbes teaches, pertaining to claim 5, a method wherein the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface (paragraph [0068]). Also, Forbes teaches, pertaining to claim 6, a method wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer to form a void in the

first silicon layer of the substrate from the first channel to the second channel produces a relaxed portion of the $Si_{1-x}Ge_x$ layer above the void (paragraph [0049]). Forbes teaches, pertaining to claims 7 and 17, a method further comprising a step of (thermal) annealing the $Si_{1-x}Ge_x$ layer after the void is formed in the first silicon layer (and before the first and second channels and the void are filled with dielectric material) (paragraphs [0048-0049] and [0056-0058]). Finally, Forbes teaches, pertaining to claim 18, a method further comprising a step of planarization after filling the first and second channels and the void with a dielectric material (paragraphs [0048-0049]).

It would have been obvious to one of ordinary skill in the art to substitute, removing a portion of the substrate (silicon layer) underneath the $Si_{1-x}Ge_x$ layer to form a void in the substrate (first silicon layer of the substrate from the first channel to the second channel); and filling the channels (first and second channels) and the void with a dielectric material, in the method of Sugii, pertaining to claims 1 and 16. In addition, it would have been obvious to one of ordinary skill in the art to substitute, wherein, the void is formed in the first silicon layer of the substrate underneath the $Si_{1-x}Ge_x$ layer extending from at least the first to the second channel, pertaining to claim 2. Also, it would have been obvious to one of ordinary skill in the art to substitute, a method wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer includes a step from the group consisting of: etching the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer; performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the substrate than for $Si_{1-x}Ge_x$; performing timed etching of the portion of the substrate underneath the Si_{1-}

$_xGe_x$ layer using an etchant from the group consisting of ammonia, tertramethyl ammonium hydroxide, nitric acid and hydrofluoric acid, pertaining to claim 3. It would have been obvious to one of ordinary skill in the art to substitute, a method wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface, pertaining to claim 4. Finally, it would have been obvious to one of ordinary skill in the art to substitute, a method wherein the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface, pertaining to claim 5, according to the teachings of Forbes, with the motivation that, by fully undercutting the rows of silicon after etching the trenches, a creation of the silicon islands that include a relaxed silicon germanium layers, results in complete isolation between the silicon-on-insulator islands. Therefore, it would be obvious to one of ordinary skill in the art to remove a portion of the substrate (silicon layer) underneath the $Si_{1-x}Ge_x$ layer to form a void in the substrate (first silicon layer of the substrate from the first channel to the second channel) and then fill the channels (first and second channels) and the void with a dielectric material, wherein the void is formed in the first silicon layer of the substrate underneath the $Si_{1-x}Ge_x$ layer extending from at least the first to the second channel, for the purpose of creating an isolation regions between devices. In addition, it would be obvious to one of ordinary skill in the art to where the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface that includes the $Si_{1-x}Ge_x$ layer having a higher concentration of Ge at the bottom surface than at the top surface, according to the teachings of Forbes, with the motivation that, it is well known that the concentration of germanium can be controlled by the ion implantation of Ge ions, therefore one of ordinary skill

in the art would conclude that the bottom surface would be resistant to etching as well as the concentration being higher at the bottom would be routine in the conventional art.

It would have been obvious to one of ordinary skill in the art to substitute, a method wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer to form a void in the first silicon layer of the substrate from the first channel to the second channel produces a relaxed portion of the $Si_{1-x}Ge_x$ layer above the void. Also It would have been obvious to one of ordinary skill in the art to substitute, a method further comprising a step of (thermal) annealing the $Si_{1-x}Ge_x$ layer after the void is formed in the first silicon layer (and before the first and second channels and the void are filled with dielectric material), in the method of Sugii, based on the combined teachings of Sugii in view of Forbes, with the motivation that, since both Sugii and Forbes teaches, the formation of a relaxed silicon germanium layer one of ordinary skill in the art would conclude that the formation of the relaxed silicon germanium layer that includes an annealing step, would prove to be equivalent since the relaxed silicon germanium layer may be formed before creating the void. Finally, It would have been obvious to one of ordinary skill in the art to substitute, a method further comprising a step of planarization after filling the first and second channels and the void with a dielectric material, in the method of Sugii, according to both the teachings of Sugii in view of Forbes, with the motivation that, both Sugii and Forbes teaches, the use of an isolation techniques, where Sugii, specifically teaches, a planarizing the filled material, to form the trench isolation region. Therefore, it would be obvious to one of ordinary skill in the art to conclude that the presence of void would not be

required, since the planarization is performed after the filling of the trenches or channels not including the void.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STACY A. WHITMORE
PRIMARY EXAMINER

Stanetta Isaac
Patent Examiner
December 6, 2004